Signal Conditioning Circuit for Synchronized Crystal Oscillators Ensemble, General Requirements

Data Sheet 1138A

AN-ASCCXX-X Series **Rev. -**

U.S. Patent Number 7,812,682

Description

The Signal Conditioning Circuit (SCC) is intended for use in the system, which requires multiple clocks in different nodes of the system to run synchronously in frequency **without master clock** along with SXO ensemble per 1138B. It takes the input signal from one of the synchronization buses, and converts/translates it into differential (complementary) output signal with PECL or LVDS logic, or single output signal with CMOS logic. It's packaged in 17x14x6 mm SMD FR4 based package.

Applications and Features for SXO ensemble with SCC

- Unlimited scalability/easily expandable
- Ideal for blade applications
- Provides a complete, system-wide clock redundancy solution
- High reliability systems with multiple synchronous clocks.
- Greatly improved system reliability
- Low Phase Noise and jitter
- No master clock, no PLL required for the system
- Eliminates additive jitter degradation associated with clock distribution
- "Hot" – swappable
- Synchronize independent of power application sequence/No special power sequence required
- Improves Phase jitter at every node
- While in sync all units exhibit identical phase noise characteristics
- Low cost
- COTS/Dual use

NEL FREQUENCY CONTROLS, INC.

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Creating a Part Number

AN - A SCC X X - X

Package code
AN 8pad 17x14 mm

Operating Voltage
A 3.3 V ± 5%

Enable Option
L Enable Low
N N/C

Output Option
L LVDS
C CMOS
P PECL

Environmental
L Contains a level of lead that is in excess of RoHS directive and is not designed for reflow
R RoHS compliant

Note: En/Dis feature may not be available with LVDS and CMOS outputs.

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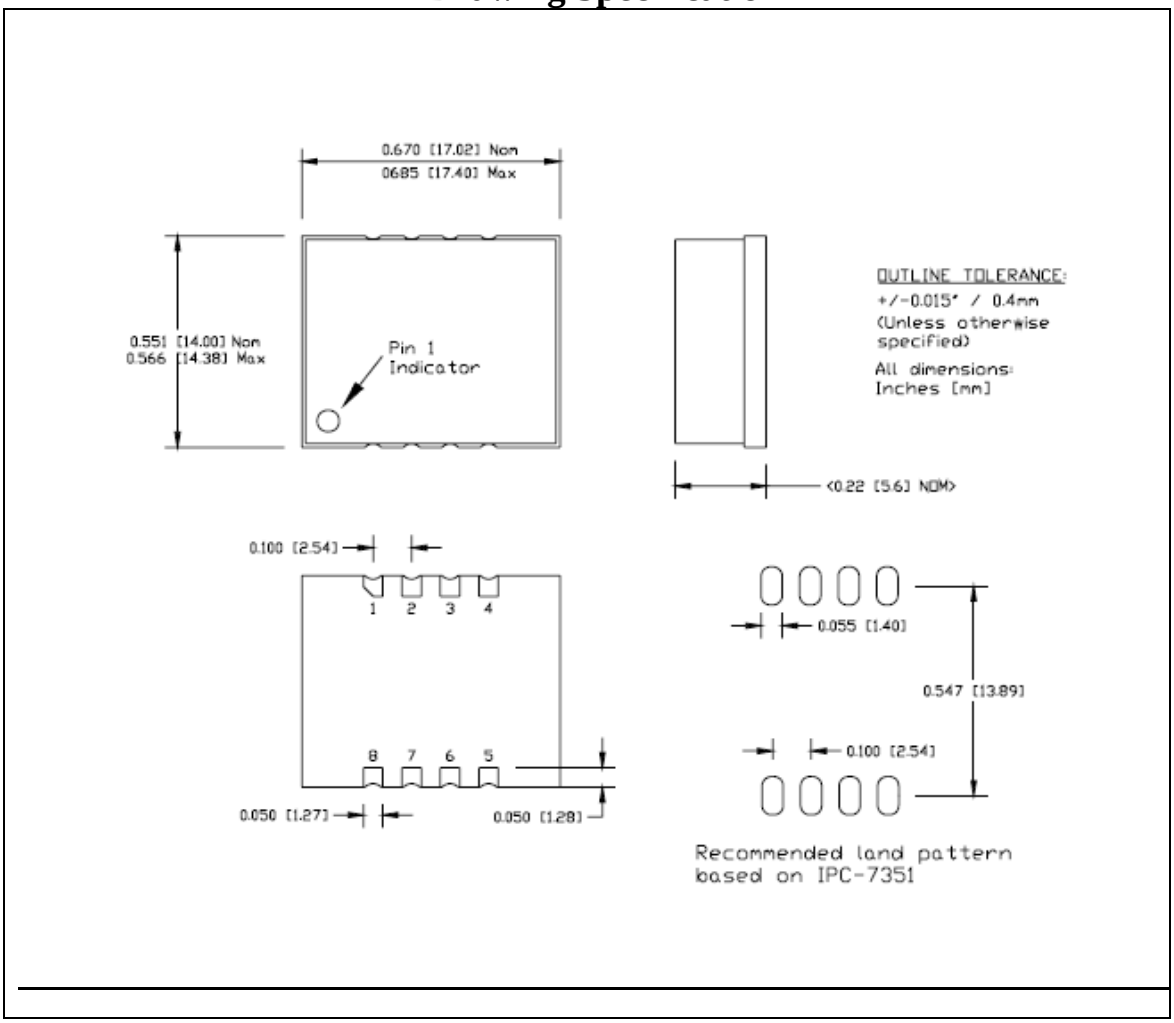
Drawing Specification



Electrical Connections

Pin out LVDS or PECL	#1 = Vcc; #2 = Sync in, ## 3, 4, 7, 8 = GND; #5 –OUT, #6 –complementary OUT
Pin out CMOS	#1 = Vcc; #2 = 100MHz in, ## 3, 4, 7, 8 = GND; #5 – CMOS OUT, #6 – N/C

Environmental and Mechanical Characteristics

Operating temp. Range	-40ºC to 85ºC
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Soldering conditions	See MAX reflow profile below

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	ºC
Storage Temperature Range	Tst	-50 to +90	ºC
Supply Voltage	Vcc	-0.5 to 3.6	V
Input Voltage Amplitude	Vin	Vcc	V

Electrical Parameters (1)

Parameter		Symb	Conditions, Note	MIN	TYP	MAX	Unit
Nominal Input Frequency		Fin		25		160	MHz
Output frequency		Fout	PECL, LVDS CMOS	25 20		800 160	MHz
Supply Voltage		Vcc		3.135	3.3	3.465	V
Supply current		Icc	Loaded both outputs,			100	mA
LVDS OUTPUT	Load		At receiving end between the outputs	90	100	120	Ohm
	Output Levels	Vod	Differential amplitude	247	330	454	mV
			Amplitude error			50	mV
		Vof	Offset Voltage	1.125	1.25	1.375	V
			Offset voltage error			50	mV
	Duty Cycle (Symmetry)		At outputs crossing, room temperature	45/55	50/50	55/45	%
	Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.3	0.5	ns
LVPECL OUTPUT	Load		Output to Vcc-2V, or Thevenin Equivalent		50		Ohm
	Output Levels	Voh Vol	Overall	Vcc-1.025		Vcc-1.620	V
	Duty Cycle (Symmetry)		At 50% of output voltage swing	45/55	50/50	55/45	%
	Rise/Fall Time	Tr,Tf	20 to 80, 80 to 20%		0.5	0.7	ns
CMOS	Load				15pf/10K ohm		Ohm
	Output Levels	Voh Vol	Overall	0.9Vcc		0.1Vcc	V
	Duty Cycle (Symmetry)		At 50% Vcc	45/55	50/50	45/55	%
	Rise/Fall Time	Tr,Tf	0.2Vcc to 0.8Vcc F<70MHz 70MHz<F<125MHz 125MHz<F<250MHz		 3 2 1.5	 5 3 2.5	ns
Input signal		Vin	Peak-to-peak	0.5		Vcc	V
Subharmonics and multiples					-55	-50	dBc
Deterministic Jitter		DJ	Peak-to-peak		0.7	1	ps
Skew			Unit to unit			2	Degrees

Note: 1. All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

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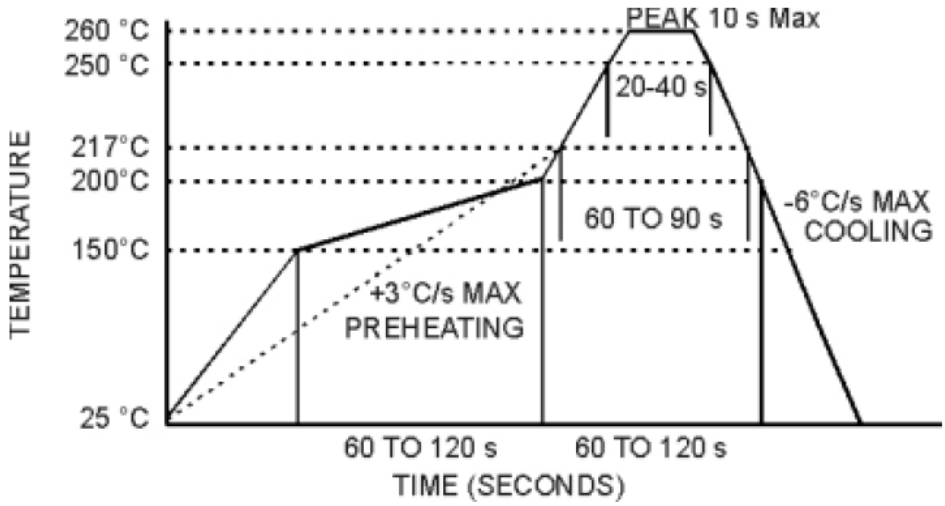
MAX Reflow Profile



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